REMARKS

(A) Claims 1 & 17 objections:

Please find the amended claims in compliance with the examiner's request. Withdrawal of the objections to claims 1, 17 and those dependent thereupon is respectfully requested.

(B) 35 USC 102 Rejections:

The applicant's disclosure pertains to a programmable device with dual memory construction options wherein the logic circuits and circuits interconnect structure remain invariant to the memory construction options. Such devices offer timing exactness with multiple memory options. Only the storage element that generates control signals is varied in these devices to achieve substantially timing exact circuit performance with either of the memory options. The amended Claim-8 now recites:

> 8. A programmable logic device (PLD) comprising two selectable memory construction options to control logic circuits, wherein:
> a first selectable option comprises a random access memory (RAM) construction; and
> a second selectable option comprises a hard-wire read only memory (ROM) construction;
> wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options.

In contrast, Duong et al. (US 5,600,264) discloses a six transistor switch box for a signal channel (ref. Abstract). The switch box 155 in Fig-2 comprises memory elements, and a plurality of programmable memory choices (Col. 4, lines 48+) are claimed to provide the desired programmability. However, the logic circuit 155 has to be modified (as illustrated by the applicant below) in order to use the listed different memory options. Thus a first PLD uses a first memory option, a second PLD uses a second memory option, etc. Thus, Duong disclosure does not pertain to logic circuits or interconnect structure that is invariant to the memory choice, nor timing exactness between multiple programmable memory choices.

On page-2, the examiner stated: "*Regarding claim 8, Duong disclosure Figs. 2 5, a programmable logic device (PLD) (col. 1, lines 12+) comprising two selectable memory construction options (col. 4, lines 48+) to control logic,..*".

A first basis to traverse the examiners rejection is that Duong does not disclose a single PLD that comprises two selectable memory constructions. To illustrate this, a first memory option of SRAM and a second memory option of EPROM are considered. With reference to Fig-2, in Col. 3, lines 61+, Duong eludes to a pass-transistor 210a, wherein the gate is coupled to memory cell 210b. The memory cell 210b in the first case is SRAM and in the second case is EPROM. The memory cell controls the state of pass-transistor: either ON or OFF (Col. 4, line 66), ON means a signal level greater than Vt (ideally Vcc), and OFF means a signal level less than the Vt (ideally Vss) for the pass-transistor 210a. In applicant's Fig-3A/B, this specific Duong illustration is shown in greater detail for the SRAM cell: further illustrating how the ON & OFF controls is achieved with an SRAM cell 350. It is clear that an ON and OFF S_0 signal levels at Vcc & Vss can be generated by the memory cell 350 due to the cross coupled inverter logic inside the SRAM cell. An EPROM cell that offers similar controls is not illustrated by Duong. An EPROM (or Flash) cell is analog in nature (due to the charge packet trapped in the floating gate) and has no propensity to generate Vcc or Vss controls for the pass gate transistor 210a to be ON or OFF. The Applicant shows an EPROM embodiment (also true for Flash) in Applicant's Fig-2D, described in page 7, line 16, wherein the Duong memory cell 210b & Duong pass gate 210a are both incorporated into a single floating-gate cell 240 to implement a switch. Clearly the second PLD is different: for SRAM, 210a is a logic NMOS transistor with standard logic gate oxide; for EPROM, 210a is a floating gate transistor with special EPROM gate oxide. The oxides have to be different as trapped charges require very strict data retention measures compared to ordinary logic control signals.

A second basis to traverse the rejection is on the grounds that Duong logic circuits do not remain invariant to the memory construction option. Again, SRAM and EPROM memory construction options are utilized to illustrate the differences. With an SRAM option, the pass gate transistor 210a and SRAM cell 210b are fabricated utilizing single poly NMOS and PMOS transistors that are arranged in a certain pattern on a Si substrate layer. The layout of NMOS and PMOS transistors require N-wells, P-wells, and well spacing rules. An optimized transistor layout arrangement must follow CMOS layout rules required to build these circuits. Assuming one knows how to construct an EPROM cell to replace the SRAM cell (which by itself would be new invented matter) an EPROM cell 210b requires a stack two poly transistor, while the NMOS 210a is a single poly transistor. There are no N-wells in this arrangement, and no N-well to P-

well spacing rules are required to arrange the EPROM cell and pass-gate transistor. However, there are stack-poly and single poly spacing rules that dictate how these must be constructed together. As a result, an SRAM cell and an EPROM cell will have completely different transistor layouts for logic circuits portion, and the ensuing interconnects that couple the logic circuits together will also differ. As a consequence, every single masking layer to construct logic circuits will differ between the SRAM based PLD and the EPROM based PLD.

The applicant respectfully traverses the anticipation rejection further as the following high lighted claim elements of Applicant's independent claims are not disclosed or taught by Duong:

Applicant's Claim-1:

"*a second selectable fabrication option comprised of a hard-wired circuit in lieu of said user configurable memory circuit*". Duong discloses programmable memory elements to fabricate PLDs, all of which are programmed during initialization (col. 4, line 58). There is no disclosure on hard-wired circuits in lieu of memory circuits as a memory option.

"*wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options*". Duong discloses a plurality of PLDs, each PLD with a unique memory option. No two Duong PLDs are claimed to have substantially identical timing characteristics.

Applicant's Claim-8:

"*a second selectable option comprises a hard-wire read only memory (ROM) construction*". Duong discloses programmable memory elements to fabricate PLDs, all of which are programmed during initialization (col. 4, line 58). There is no disclosure of hard-wired ROM as a memory option.

"*wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options*". Duong discloses a plurality of PLDs, each PLD with a unique memory option. Each PLD further comprises a unique logic circuit pattern. No two Duong PLDs are claimed to have logic circuit masking patterns invariant to memory options.

Applicant's Claim-17:

"*wherein the memory element construction comprises; a second selectable option comprising a hard-wire read only memory (ROM) construction*". Duong discloses programmable memory elements to fabricate PLDs, all of which are programmed during initialization (col. 4, line 58). There is no disclosure on hard-wired ROM as a memory option.

"*wherein, the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options*". Duong discloses a plurality of PLDs, each PLD with a unique memory option. Each PLD further comprises a unique pass-gate logic element masking pattern. No two Duong PLDs are claimed to have pass-gate logic element masking patterns invariant to memory options.

The applicant respectfully traverses the anticipation rejection as the following motivations are not disclosed by Duong:

The motivation for the ROM replacement of RAM is to achieve: (a) better reliability by eliminating RAM elements (page 13, line 6-9)), (b) lower cost due to higher ROM yield compared to RAM (page 13, line 6-9, also pages 28-31) (c) conversion of volatile RAM data to nonvolatile ROM data (page 12, line 2-4), (d) timing exact design conversions to a lower cost device (page 9, line 14-15), and (e) no re-qualification requirements for the conversion (page 13, line 17).

In contrast, the motivation for Duong invention is to provide a buffered signal to reduce the pass transistor related RC delay (col. 2, line 19-25). There is no motivation in Duong to obtain a timing exact lower cost solution to an expensive programmable device.

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
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> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The applicant believes that each of the independent claims (Claim 1, 8 & 17) in the current application comprises a plurality of claim elements that are expressly or impliedly not described by Duong. Furthermore, Duong fails to provide a motivation for one with ordinary skill to realize the Applicant's disclosure as stated in the claim elements. The applicant believes that the independent claims and those dependent thereupon (Claims 1-20) are not anticipated by Duong. Withdrawal of the rejections of claims 1-20 is respectfully requested.

CONCLUSION

Applicant believes that the above discussion is fully responsive to all grounds of objections and rejections set forth in the Office Action.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868, or cell phone (408) 431-5367.

Respectfully submitted,

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